Exhibit D

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Request for Continued Examination (RCE) Transmittal

Address to:
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P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	17/196,665-Conf. #8466
Filing Date	March 9, 2021
First Named Inventor	Thomas Lippert
Art Unit	2441
Examiner Name	O. Duong
Attorney Docket Number	29959/51333B

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).
   - a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
     - i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
     - ii. ☐ Other _____
   - b. ☒ Enclosed
     - i. ☒ Amendment/Reply
     - ii. ☐ Affidavit(s)/ Declaration(s)
     - iii. ☐ Information Disclosure Statement (IDS)
     - iv. ☐ Other _____
2. Miscellaneous
   - a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
   - b. ☐ Other _____
3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
   - a. ☒ The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 13-2855 .
     - i. ☒ RCE fee required under 37 CFR 1.17(e)
     - ii. ☒ Extension of time fee (37 CFR 1.136 and 1.17)
     - iii. ☐ Other _____
   - b. ☐ Check in the amount of $ _____ enclosed
   - c. ☒ Payment by credit card ~~(Form PTO-2038 enclosed)~~
   - d. ☒ Payment by EFS-Web

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Matthew R. Carey/	Date	August 24, 2022
Name (Print/Type)	Matthew R. Carey	Registration No.	61,082

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being EFS-Web transmitted to the United States Patent and Trademark Office (USPTO), deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the USPTO on the date shown below.

Signature			
Name (Print/Type)		Date	

Docket No.: 29959/51333B
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Thomas Lippert

Application No.: 17/196,665 | Confirmation No.: 8466

Filed: March 9, 2021 | Art Unit: 2441

For: COMPUTER CLUSTER ARRANGEMENT FOR PROCESSING A COMPUTATION TASK AND METHOD FOR OPERATION THEREOF | Examiner: O. Duong

AMENDMENT IN RESPONSE TO FINAL OFFICE ACTION, ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION

MS RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

INTRODUCTORY COMMENTS

In response to the Final Office Action dated May 4, 2022:

Listing of the Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 5 of this paper.

LISTING OF THE CLAIMS

1. (Original) A computer cluster system for processing a computation task, comprising:

a plurality of hardware computation nodes, a plurality of hardware boosters, and a resource manager, the plurality of hardware computation nodes and the plurality of hardware boosters each interfacing a communication infrastructure;

the resource manager being arranged to assign a selected hardware booster of the plurality of hardware boosters to a first hardware computation node of the plurality of hardware computation nodes for computation of a part of the computation task, and

wherein the resource manager is arranged to provide assignment information to the first hardware computation node after the assignment of the selected hardware booster so as to enable the first hardware computation node to output the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node.

2. (Original) The computer cluster system according to claim 1, wherein the resource manager is arranged to perform said assignment of the selected hardware booster to the first hardware computation node as a function of a predetermined assignment metric, the assignment being static at a start of processing of the computation task and a dynamic assignment during processing of the computation task.

3. (Original) The computer cluster system according to claim 2, wherein the resource manager is arranged to perform the dynamic assignment in response to specific computation task characteristics.

4. (Original) The computer cluster system according to claim 2, wherein said predetermined assignment metric is formed according to at least one of a group of metric specification techniques, said group of metric specification techniques comprising: a temporal logic, an assignment matrix, an assignment table, a probability function, and a cost function.

5. (Original) The computer cluster system according to claim 2, wherein said predetermined assignment metric is specified as a function of at least one of a group of assignment parameters, said group of assignment parameters comprising: resource

information, cost information, complexity information, scalability information, a computation log record, compiler information, priority information, and a time stamp.

6. (Original) The computer cluster system according to claim 1, wherein said assignment of the selected hardware booster to the first hardware computation node triggers at least one of a group of signals, said group of signals comprising: a remote procedure call, a parameter handover, and a data transmission.

7. (Original) The computer cluster system according to claim 1, wherein each hardware computation node of the plurality of hardware computation nodes and each hardware booster of the plurality of hardware boosters respectively interfaces said communication infrastructure via an interfacing unit.

8. (Original) The computer cluster system according to claim 7, wherein said interfacing unit comprises at least one of a group of components, said group of components comprising: a virtual interface, a stub, a socket, a network controller, and a network device.

9. (Original) The computer cluster system according to claim 1, wherein said communication infrastructure comprises at least one of a group of components, said group of components comprising: a bus, a communication link, a switching unit, a router, and a high speed network.

10. (Original) The computer cluster system according to claim 1, wherein each hardware computation node of the plurality of hardware computation nodes comprises at least one of a group of components, said group comprising: a multi-core processor, a cluster, a computer, a workstation, and a multi purpose processor.

11. (Original) The computer cluster system according to claim 1, wherein said selected hardware booster comprises at least one of a group of components, said group of components comprising: a many-core processor, a scalar processor, a co-processor, a graphical processing unit, a cluster of many-core processors, and a monolithic processor.

12. (Original) The computer cluster system according to claim 2, wherein said resource manager is arranged to update said predetermined assignment metric during computation of said computation task.

13. (Original) The computer cluster system according to claim 1, wherein the resource manager is arranged to detect computing capacities of the plurality of hardware boosters and computation task requirements of a hardware computation node of the plurality of hardware computation nodes, and to perform an assignment of a selected one or more hardware boosters of the plurality of hardware boosters to provide required capacities to the hardware computation node.

14. (Original) A method for operating a computer cluster arrangement for processing a computation task, comprising:

computing at least a first part of a computation task by at least two of a plurality of computation nodes, each computation node of the plurality of computation nodes interfacing a communication infrastructure;

assigning a selected booster of a plurality of boosters to a first computation node of the plurality of computation nodes by a resource manager, for computation of a second part of said computation task, said assignment being accomplished as a function of a predetermined assignment metric wherein the resource manager provides assignment information to the first computation node after the assignment of the selected booster enabling the first computation node to output the second part of the computation task to the assigned selected booster under control of the first computation node.

15. (Original) The method of claim 14, wherein the first computation node is included in the at least one computation node.

REMARKS

Claims 1-15 are pending in the present application.

From the Final Office Action (FOA) dated May 4, 2022, claims 1-15 stand rejected under 35 U.S.C. 102 as allegedly being anticipated by Krishnamurthy et al. (US 2012/0054770; hereinafter "Krishnamurthy"). In view of the foregoing amendments and the following remarks, reconsideration and allowance are respectfully requested.

Claim Rejection Under 35 U.S.C. § 102

Claims 1-15 stand rejected under 35 U.S.C. § 102 as allegedly being anticipated by Krishnamurthy. Applicant respectfully traverses the rejection because Krishnamurthy fails to disclose each and every element of the claims.

Claim 1 recites a computer cluster system for processing a computation task comprising, *inter alia*, "the resource manager being arranged to assign a selected hardware booster of the plurality of hardware boosters to a first hardware computation node of the plurality of hardware computation nodes for computation of a part of the computation task," and "wherein the resource manager is arranged to provide assignment information to the first hardware computation node after the assignment of the selected hardware booster so as to enable the first hardware computation node to output the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node." Claim 14 recites similar elements. Applicant respectfully submits that Krishnamurthy fails to disclose at least this combination of elements.

Computation notes vs. boosters

As a threshold matter, the present application as well as the claims differentiate between boosters and computation nodes. Paragraph [0011] of the present application refers to boosters as accelerators ("a sharing of accelerators, here in form of boosters"). Further, the terms "computation nodes" and "boosters/accelerators" are technical terms in the field of (high performance) computing which have a clear and unambiguous meaning, in particular with regard to their technical design and configuration. A further definition of the design is also given in paragraph [0027]: "Processors being applied in boosters typically comprise an extensive arithmetic logic unit and a simple control structure when being compared to computation nodes processors." Paragraph [0073] references Intel's many-core processor Knight's Corner and Knight's Ferry as an example of a booster.

Krishnamurthy also refers to the concept of accelerators and host computers/server systems with corresponding processors. As described in paragraphs [0003], [0025], and [0029] of Krishnamurthy, host computers and accelerators have different architectures,

wherein the accelerator architecture is optimized with respect to the service system for speed of execution of a particular class of computing functions. Due to the differences in hardware architecture, computer program instructions compiled for execution on the processors of a server system generally would not be expected to execute natively on the processor of an accelerator.

Server systems and accelerators support different instruction sets, as indicated by the example in paragraph [0025] of Krishnamurthy naming the IBM System z processor for host computers and the IBM POWER instruction set implemented by architectural registers of accelerators.

Bearing in mind the meaning of the technical terms “host computer/computer nodes” in combination with “accelerators/boosters” as described in Krishnamurthy, a person having ordinary skill in the art would not equate the accelerators 104 of Krishnamurthy with the hardware computation nodes of claims 1 and 14 or the server systems 102 of Krishnamurthy with the boosters of claims 1 and 14, as is asserted in the FOA. Instead, a person having ordinary skill in the art would equate accelerators with boosters and hardware computation nodes with server systems. Therefore, the FOA employs improper technical meanings of these claimed technical terms.

Assignment

Regarding the claimed features of “the resource manager being arranged to assign a selected hardware booster of the plurality of hardware boosters to a first hardware computation node of the plurality of hardware computation nodes for computation of a part of the computation task, and wherein the resource manager is arranged to provide assignment information to the first hardware computation node after the assignment of the selected hardware booster so as to enable the first hardware computation node to output the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node,” the FOA asserts a new alleged disclosure in Krishnamurthy of said features. Applicant respectfully disagrees with these assertion.

The assignment and outsourcing/output of a part of the computation task is a two-step procedure which is clearly defined in independent claims 1 and 14. First, the resource manager assigns a selected hardware booster to a first computation node. Accordingly, this assignment is an assignment of two entities within the system. Subsequently, the assignment information is provided to the first hardware combination node, i.e., to the first hardware computation node to which the booster is assigned.

In the second step, the first hardware computation node uses said assignment information to outsource a part of the computation task from the first hardware computation

node to the assigned booster. The claim language clearly defines that the part of the computation task is moved **from** the first hardware computation node **to** the assigned booster ("the hardware computation node **to output** the part of the computation task to the assigned selected hardware booster" – emphasis added).

A further limitation is that the output/outsourcing is performed "under control of the first hardware computation node." Accordingly, after the assignment is performed by the resource manager, the fist hardware computation node can make use of the assignment and outsource parts of the computation tasks to the assigned boosters (without further need to implicate the resource manager).

Indeed, Krishnamurthy fails to disclose an assignment of server systems and accelerators and, accordingly, also fails to disclose the two-step arrangement of outsourcing parts of computation tasks. Instead, Krishnamurthy (and particularly the newly cited paragraphs [0038]-[0040]) disclose an "assignment" of tasks to server/accelerator processors.

The process described in paragraph [0039] in Krishnamurthy is used when the accelerators cannot satisfy the SLA requirements. In this case, the workload manager schedules a portion of the accelerator workload to so-called surrogate processors. At best, this is an assignment of workload/tasks to surrogate processors/server processors and not an assignment of entities like server system processors to accelerators/accelerator processors. Accordingly, Krishnamurthy fails to disclose the assignment functionality as recited in claims 1 and 14.

With regard to the claimed feature "output the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node," the FOA asserts, from the disclosure of paragraphs [0038] to [0040] of Krishnamurthy, that the workload manager 118 dynamically allocates/provides additional kernels 206, 208, 214, 216 to the server system 102, accelerators 104, or both so that additional accelerator workloads can be executed. Applicant respectfully disagrees with this assertion for multiple reasons.

First, the allocation of kernels cannot be considered to be equal to "provide assignment information to the first hardware computation node," as recited in claims 1 and 14. Assignment information is information about the assignment, i.e., the assignment of a booster to the computation node, so that the computation node is aware of which boosters are assigned. Instead, according to Krishnamurthy, kernels are sent, which are considered to be sub-tasks.

Second, claims 1 and 14 require that the first hardware computation node to which the assignment information is provided, itself outputs a part of the computation task. In contrast, the server system and accelerators of Krishnamurthy which receive the kernels – which the FOA considers to be the assignment information - also receive the additional workload.

Third, the output of the part of the computation task is not done under the control of the first hardware computation node, i.e., the hardware computation node which receives assignment information. Instead, according to Krishnamurthy, the workload manager dynamically allocates/provides additional kernels to the server systems/accelerators.

Accordingly, the system described in Krishnamurthy is completely different from the claimed features. One advantage of the present invention is that after a booster has been assigned to a computation node, the computation node can make use of the booster and outsource parts of the computation tasks to the booster under said assignment. Such an outsourcing can be done repeatedly under the assignment.

For at least these reasons, Krisnamurth fails to disclose the claimed combination "the resource manager being arranged to assign a selected hardware booster of the plurality of hardware boosters to a first hardware computation node of the plurality of hardware computation nodes for computation of a part of the computation task," and "wherein the resource manager is arranged to provide assignment information to the first hardware computation node after the assignment of the selected hardware booster so as to enable the first hardware computation node to output the part of the computation task to the assigned selected hardware booster under control of the first hardware computation node," as recited in claims 1 and as similarly recited in claim 14. Therefore, Krishnamurthy fails to anticipate claims 1 and 14.

Accordingly, Applicant respectfully submits that the rejection of claims 1 and 14 under 35 U.S.C. § 102 is overcome and requests that the rejection be withdrawn. Further, claims 2-13 and 15 depend from either claim 1 or 14. Therefore, the rejection of these claims should be withdrawn for at least the reasons mentioned below.

CONCLUSION

In view of the above, Applicant submits the pending application is in condition for allowance and an early action so indicating is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855, under Order No. 29959/51333B, from which the undersigned is authorized to draw.

Dated: August 24, 2022

Respectfully submitted,

By__/Matthew R. Carey/_____
Matthew R. Carey
Registration No.: 61,082
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive
6300 Willis Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant

Electronic Patent Application Fee Transmittal

Application Number:	17196665
Filing Date:	09-Mar-2021
Title of Invention:	COMPUTER CLUSTER ARRANGEMENT FOR PROCESSING A COMPUTATION TASK AND METHOD FOR OPERATION THEREOF
First Named Inventor/Applicant Name:	Thomas Lippert
Filer:	Matthew Richard Carey/Jacquelin Garcia
Attorney Docket Number:	29959/51333B

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	2251	1	110	110
Miscellaneous:				
RCE- 1ST REQUEST	2801	1	680	680
		Total in USD ($)		**790**